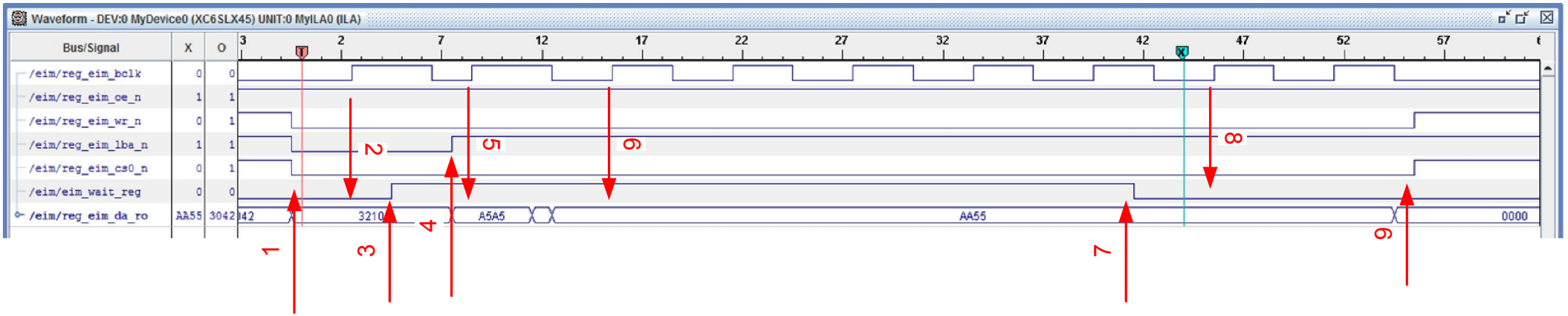

Here is what WRITE transaction looks like. Wait flag is shown using positive logic, it is inverted in actual hardware.

1. Chip Select is asserted, write flag is asserted, LBA is asserted.

2. First databeat takes place, arbiter latches address as LBA is asserted and understands that write transaction is initiated, because write flag is asserted.

3. Arbiter asserts wait flag.

4. LBA flag is cleared, meaning that next databeat will contain data, not address.

5. Second databeat takes place, arbiter latches lower bits of data.

6. Third databeat takes place, arbiter latches higher bits of data, glues everything together, sends address and data to user-side logic and starts waiting for an acknowledge signal.

7. Arbiter received acknowledge signal from user-side logic and cleared wait flag.

8. Master detected that wait flag was cleared.

9. Chip Select is cleared, transaction finished.